

Encounter Conformal Equivalence Checker

Formal verification technology for fast and accurate bug detection and correction

Cadence® Encounter® Conformal® Equivalence Checker (EC) makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the industry's only complete equivalence checking solution for verifying SoC designs—from RTL to final LVS-netlist (SPICE)—as well as FPGA designs. Encounter Conformal EC enables designers to verify the widest variety of circuits, including complex arithmetic logic, datapaths, memories, and custom logic.

Encounter Conformal EC

Already proven in thousands of tapeouts, Encounter Conformal EC is the industry's most widely supported independent equivalence checking product. It is production-proven on more physical design closure products, advanced synthesis software, ASIC libraries, and IP cores than any other formal verification technology.

Encounter Conformal EC is available in three configurations: the L offering delivers gate equivalence checking technology; the XL offering extends the L capabilities with automated checking of complex datapaths; and equivalence checking at the final place-and-route netlist; the QOL offering extends the L and XL capabilities with transistor circuit analysis for custom designs and embedded memories.

Engineers can use the QOL offering with custom embedded memories, arithmetic blocks, datapaths, mixed and extended libraries, and all other custom and semi-custom digital circuit functions. Circuit styles supported include standard and complex Boolean functions, latches and registers, pass-gates, transmission-gates, tri-state switch logic, pre-charged logic cells, domino logic blocks, and dual-rail.

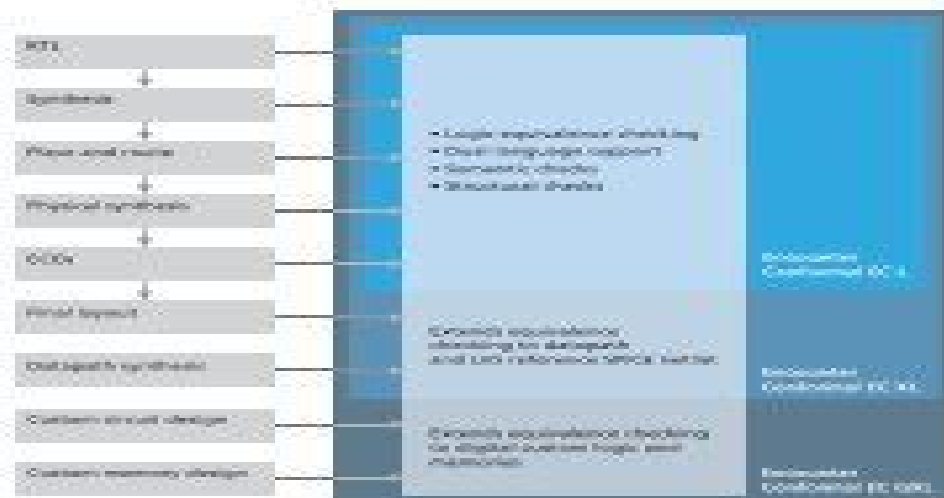


Figure 1. Encounter Conformal EC offers a complete solution, from RTL to final layout, to affine convergence on design goals.

Cadence Conformal Lec User Guide

Burton Paul



Cadence Conformal Lec User Guide:

A Practical Approach to VLSI System on Chip (SoC) Design Veena S. Chakravarthi, 2019-09-25 This book provides a comprehensive overview of the VLSI design process. It covers end to end system on chip SoC design including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF based low power design flow issues for deep submicron SOC designs which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade and will also be a valuable professional reference for those already working in VLSI design and verification with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers. Covers end to end VLSI SoC design flow. Includes source code, case studies, and application examples.

User's Manual for Program CONFORM (CONFORMal Contact Stress Problems). Burton Paul, 1978

Unveiling the Magic of Words: A Report on "**Cadence Conformal Lec User Guide**"

In a global defined by information and interconnectivity, the enchanting power of words has acquired unparalleled significance. Their power to kindle emotions, provoke contemplation, and ignite transformative change is actually awe-inspiring. Enter the realm of "**Cadence Conformal Lec User Guide**," a mesmerizing literary masterpiece penned by way of a distinguished author, guiding readers on a profound journey to unravel the secrets and potential hidden within every word. In this critique, we shall delve to the book is central themes, examine its distinctive writing style, and assess its profound affect the souls of its readers.

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