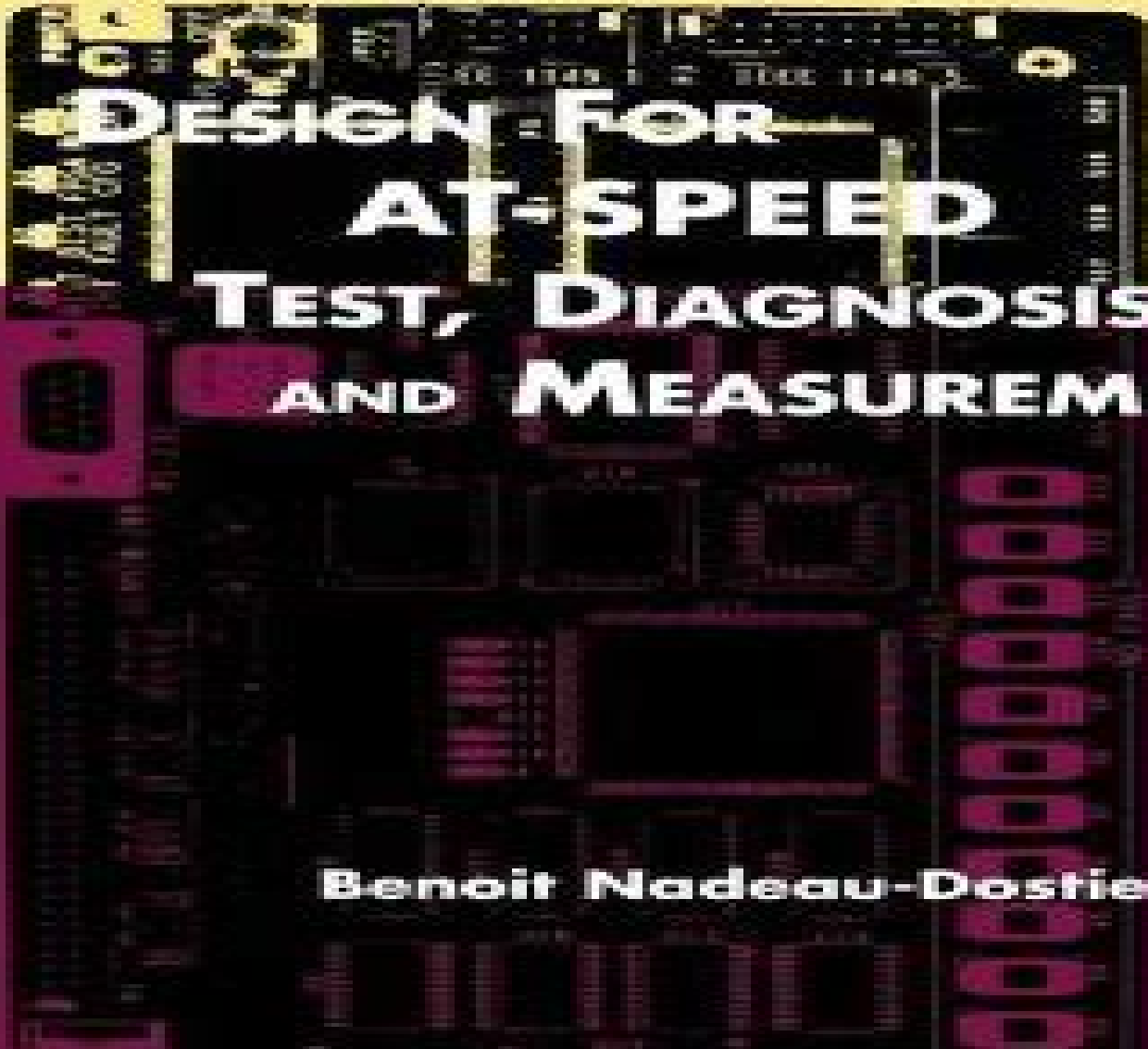




# **DESIGN FOR AT-SPEED TEST, DIAGNOSIS AND MEASUREMENT**

**Benoit Nadeau-Dostie**

# Design For At Speed Test Diagnosis And Measurement

**Charles E. Stroud**



## **Design For At Speed Test Diagnosis And Measurement:**

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Design for AT Speed Test Diagnosis and Measurement is the first book to offer practical and proven design for testability DFT solutions to chip and system design engineers test engineers and product managers at the silicon level as well as at the board and systems levels Designers will see how the implementation of embedded test enables simplification of silicon debug and system bring up Test engineers will determine how embedded test provides a superior level of at speed test diagnosis and measurement without exceeding the capabilities of their equipment Product managers will learn how the time resources and costs associated with test development manufacture cost and lifecycle maintenance of their products can be significantly reduced by designing embedded test in the product A complete design flow and analysis of the impact of embedded test on a design makes this book a must read before any DFT is attempted

**Introduction to Advanced System-on-Chip Test Design and Optimization** Erik Larsson, 2006-03-30

SOC test design and its optimization is the topic of Introduction to Advanced System on Chip Test Design and Optimization It gives an introduction to testing describes the problems related to SOC testing discusses the modeling granularity and the implementation into EDA electronic design automation tools The book is divided into three sections i test concepts ii SOC design for test and iii SOC test applications The first part covers an introduction into test problems including faults fault types design flow design for test techniques such as scan testing and Boundary Scan The second part of the book discusses SOC related problems such as system modeling test conflicts power consumption test access mechanism design test scheduling and defect oriented scheduling Finally the third part focuses on SOC applications such as integrated test scheduling and TAM design defect oriented scheduling and integrating test design with the core selection process

*VLSI Test Principles and Architectures* Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, 2006-08-14

This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures

**A Designer's Guide to Built-In Self-Test** Charles E. Stroud, 2005-12-27

A recent technological advance is the art of designing circuits to test themselves referred to as a Built In Self Test This book is written from a designer's perspective and describes the major BIST approaches that have been proposed and implemented along with their advantages and limitations

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits M. Bushnell, Vishwani Agrawal, 2006-04-11

The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on

testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device technology circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signal subsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers

**Electronic Design Automation** Laung-Terng Wang, Yao-Wen Chang, Kwang-Ting (Tim) Cheng, 2009-03-11 This book provides broad and comprehensive coverage of the entire EDA flow EDA VLSI practitioners and researchers in need of fluency in an adjacent field will find this an invaluable reference to the basic EDA concepts principles data structures algorithms and architectures for the design verification and test of VLSI circuits Anyone who needs to learn the concepts principles data structures algorithms and architectures of the EDA flow will benefit from this book Covers complete spectrum of the EDA flow from ESL design modeling to logic test synthesis verification physical design and test helps EDA newcomers to get up and running quickly Includes comprehensive coverage of EDA concepts principles data structures algorithms and architectures helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books including Test compression ESL design modeling large scale floorplanning placement routing synthesis of clock and power ground networks helps readers to design develop testable chips or products Includes industry best practices wherever appropriate in most chapters helps readers avoid costly mistakes     SOC (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty, 2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOC is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing     System-on-Chip Test Architectures Laung-Terng

Wang, Charles E. Stroud, Nur A. Touba, 2010-07-28 Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly. System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs. Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations and examples. Most up to date coverage available including Fault Tolerance, Low Power Testing, Defect and Error Tolerance, Network on Chip, NOC Testing, Software Based Self Testing, FPGA Testing, MEMS Testing, and System In Package, SIP Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era, promising nanotechnology test techniques including Quantum Dots, Cellular Automata, Carbon Nanotubes, and Hybrid Semiconductor Nanowire Molecular Computing. Practical problems at the end of each chapter for students. *Power-Constrained Testing of VLSI Circuits* Nicola Nicolici, Bashir M. Al-Hashimi, 2006-04-11 This text focuses on techniques for minimizing power dissipation during test application at logic and register transfer levels of abstraction of the VLSI design flow. It surveys existing techniques and presents several test automation techniques for reducing power in scan based sequential circuits and BIST data paths.

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