

David S. Hardin
Editor

Design and Verification of Microprocessor Systems for High-Assurance Applications

 Springer

Design And Verification Of Microprocessor Systems For High Assurance Applications

Jakub Szefer



Design And Verification Of Microprocessor Systems For High Assurance Applications:

Design and Verification of Microprocessor Systems for High-Assurance Applications David S. Hardin, 2010-03-02 Microprocessors increasingly control and monitor our most critical systems including automobiles airliners medical systems transportation grids and defense systems The relentless march of semiconductor process technology has given engineers exponentially increasing transistor budgets at constant recurring cost This has encouraged increased functional integration onto a single die as well as increased architectural sophistication of the functional units themselves Additionally design cycle times are decreasing thus putting increased schedule pressure on engineers Not surprisingly this environment has led to a number of uncaught design flaws Traditional simulation based design verification has not kept up with the scale or pace of modern microprocessor system design Formal verification methods offer the promise of improved bug finding capability as well as the ability to establish functional correctness of a detailed design relative to a high level specification However widespread use of formal methods has had to await breakthroughs in automated reasoning integration with engineering design languages and processes scalability and usability This book presents several breakthrough design and verification techniques that allow these powerful formal methods to be employed in the real world of high assurance microprocessor system design

Tools and Algorithms for the Construction and Analysis of Systems Bernd Finkbeiner, Laura Kovács, 2024-04-03 The open access book 3 volume set LNCS 14570 14573 constitutes the proceedings of the 30th International Conference on Tools and Algorithms for the Construction and Analysis of Systems TACAS 2024 which was held as part of the European Joint Conferences on Theory and Practice of Software ETAPS 2024 during April 6 11 2024 in Luxembourg The 53 full papers and 16 short SVComp contributions included in these proceedings were carefully reviewed and selected from 159 submissions They were organized in topical sections as follows Part I STA and SMT solving synthesis logic and decidability program analysis and proofs proof checking Part II Model Checking automata and learning software verification probabilistic systems simulations Part III Neural networks testing and verification games concurrency SV Comp 2024

Certified Programs and Proofs Georges Gonthier, Michael Norrish, 2013-12-11 This book constitutes the refereed proceedings of the Third International Conference on Certified Programs and Proofs CPP 2013 colocated with APLAS 2013 held in Melbourne Australia in December 2013 The 18 revised regular papers presented together with 1 invited lecture were carefully reviewed and selected from 39 submissions The papers are organized in topical sections on code verification elegant proofs proof libraries certified transformations and security

Model Checking Software Owolabi Legunsen, Grigore Rosu, 2022-08-22 This book constitutes the refereed proceedings of the 28th International Symposium on Model Checking Software SPIN 2022 held virtually in May 2022 The 8 full papers were carefully reviewed and selected from 11 submissions Topics covered include formal verification techniques for automated analysis of software formal analysis for modeling languages such as UML state charts formal specification languages temporal logic design by contract model checking

automated theorem proving including SAT and SMT verifying compilers abstraction and symbolic execution techniques and much more **Leveraging Applications of Formal Methods, Verification and Validation. Modeling** Tiziana

Margaria, Bernhard Steffen, 2018-10-28 The four volume set LNCS 11244 11245 11246 and 11247 constitutes the refereed proceedings of the 8th International Symposium on Leveraging Applications of Formal Methods Verification and Validation ISoLA 2018 held in Limassol Cyprus in October November 2018 The papers presented were carefully reviewed and selected for inclusion in the proceedings Each volume focusses on an individual topic with topical section headings within the volume Part I Modeling Towards a unified view of modeling and programming X by construction STRESS 2018 Part II Verification A broader view on verification from static to runtime and back evaluating tools for software verification statistical model checking RERS 2018 doctoral symposium Part III Distributed Systems rigorous engineering of collective adaptive systems verification and validation of distributed systems and cyber physical systems engineering Part IV Industrial Practice runtime verification from the theory to the industry practice formal methods in industrial practice bridging the gap reliable smart contracts state of the art applications challenges and future directions and industrial day Principles of Secure Processor Architecture Design Jakub Szefer, 2022-06-01

With growing interest in computer security and the protection of the code and data which execute on commodity computers the amount of hardware security features in today s processors has increased significantly over the recent years No longer of just academic interest security features inside processors have been embraced by industry as well with a number of commercial secure processor architectures available today This book aims to give readers insights into the principles behind the design of academic and commercial secure processor architectures Secure processor architecture research is concerned with exploring and designing hardware features inside computer processors features which can help protect confidentiality and integrity of the code and data executing on the processor Unlike traditional processor architecture research that focuses on performance efficiency and energy as the first order design objectives secure processor architecture design has security as the first order design objective while still keeping the others as important design aspects that need to be considered This book aims to present the different challenges of secure processor architecture design to graduate students interested in research on architecture and hardware security and computer architects working in industry interested in adding security features to their designs It aims to educate readers about how the different challenges have been solved in the past and what are the best practices i e the principles for design of new secure processor architectures Based on the careful review of past work by many computer architects and security researchers readers also will come to know the five basic principles needed for secure processor architecture design The book also presents existing research challenges and potential new research directions Finally this book presents numerous design suggestions as well as discusses pitfalls and fallacies that designers should avoid **Provably Correct Systems**

Mike Hinchey, Jonathan P. Bowen, Ernst-Rüdiger Olderog, 2017-03-01 As computers increasingly control the systems and

services we depend upon within our daily lives like transport communications and the media ensuring these systems function correctly is of utmost importance This book consists of twelve chapters and one historical account that were presented at a workshop in London in 2015 marking the 25th anniversary of the European ESPRIT Basic Research project ProCoS Provably Correct Systems The ProCoS I and II projects pioneered and accelerated the automation of verification techniques resulting in a wide range of applications within many trades and sectors such as aerospace electronics communications and retail The following topics are covered An historical account of the ProCoS project Hybrid Systems Correctness of Concurrent Algorithms Interfaces and Linking Automatic Verification Run time Assertions Checking Formal and Semi Formal Methods Provably Correct Systems provides researchers designers and engineers with a complete overview of the ProCoS initiative past and present and explores current developments and perspectives within the field

Interactive Theorem Proving Gerwin Klein, Ruben Gamboa, 2014-06-28 This book constitutes the proceedings of the 5th International Conference on Interactive Theorem Proving ITP 2014 Held as Part of the Vienna Summer of Logic VSL 2014 in Vienna Austria in July 2014 The 35 papers presented in this volume were carefully reviewed and selected from 59 submissions The topics range from theoretical foundations to implementation aspects and applications in program verification security and formalization of mathematics

Theory and Applications of Satisfiability Testing -- SAT 2015 Marijn Heule, Sean Weaver, 2015-09-17 This book constitutes the refereed proceedings of the 18th International Conference on Theory and Applications of Satisfiability Testing SAT 2015 held in Austin TX USA in September 2015 The 21 regular papers 2 short papers and 7 tool papers presented together with 3 invited talks were carefully reviewed and selected from 70 submissions The papers address different aspects of SAT including theoretical advances exact algorithms proof complexity and other complexity issues practical search algorithms knowledge compilation implementation level details of SAT solvers and SAT based systems problem encodings and reformulations and applications as well as case studies and reports on insightful findings based on rigorous experimentation The paper Constructing SAT Filters with a Quantum Annealer is published open access under a CC BY NC 2.5 license at link.springer.com

Formal Verification of Floating-Point Hardware Design David M. Russinoff, 2018-10-13 This is the first book to focus on the problem of ensuring the correctness of floating point hardware designs through mathematical methods Formal Verification of Floating Point Hardware Design advances a verification methodology based on a unified theory of register transfer logic and floating point arithmetic that has been developed and applied to the formal verification of commercial floating point units over the course of more than two decades during which the author was employed by several major microprocessor design companies The book consists of five parts the first two of which present a rigorous exposition of the general theory based on the first principles of arithmetic Part I covers bit vectors and the bit manipulation primitives integer and fixed point encodings and bit wise logical operations Part II addresses the properties of floating point numbers the formats in which they are encoded as bit vectors and the various modes of floating

point rounding In Part III the theory is extended to the analysis of several algorithms and optimization techniques that are commonly used in commercial implementations of elementary arithmetic operations As a basis for the formal verification of such implementations Part IV contains high level specifications of correctness of the basic arithmetic instructions of several major industry standard floating point architectures including all details pertaining to the handling of exceptional conditions Part V illustrates the methodology applying the preceding theory to the comprehensive verification of a state of the art commercial floating point unit All of these results have been formalized in the logic of the ACL2 theorem prover and mechanically checked to ensure their correctness They are presented here however in simple conventional mathematical notation The book presupposes no familiarity with ACL2 logic design or any mathematics beyond basic high school algebra It will be of interest to verification engineers as well as arithmetic circuit designers who appreciate the value of a rigorous approach to their art and is suitable as a graduate text in computer arithmetic

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