True dependencies S4 and S3 through A[i] S2 and S1 through T[i]

- c. There is an anti-dependence between iteration i and i+1 for array B. This can be avoided by renaming the B array in S2.
- 4.15 a. Branch divergence: causes SIMD lanes to be masked when threads follow different control paths
 - Covering memory latency: a sufficient number of active threads can hide memory latency and increase instruction issue rate
 - Coalesced off-chip memory references: memory accesses should be organized consecutively within SIMD thread groups
 - d. Use of on-chip memory: memory references with locality should take advantage of on-chip memory, references to on-chip memory within a SIMD thread group should be organized to avoid bank conflicts
- 4.16 This GPU has a peak throughput of 1.5 × 16 × 16 = 384 GFLOPS/s of single-precision throughput. However, assuming each single precision operation requires four-byte two operands and outputs one four-byte result, sustaining this throughput (assuming no temporal locality) would require 12 bytes/FLOP × 384 GFLOPs/s = 4.6 TB/s of memory bandwidth. As such, this throughput is not sustainable, but can still be achieved in short bursts when using on-chip memory.
- 4.17 Reference code for programming exercise:

#include <stdio.b> #include <stdlib.h> #include <sys/time.h> #include <cuda.h> global void life (unsigned char "d board, int iterations) (int i.row.col.rows.cols; unsigned char state, neighbors: row = blockIdx.y * blockDim.y + threadIdx.y; col = blockIdx.x * blockDim.x + threadIdx.x; rows = gridDim.y * blockDim.y: cols = gridDim.x * blockDim.x: state = d board[(row)*cols+(col)]; for (i=0:i<iterations:i++) (neighbors=0; if (row!-0) { if (col!=0) if (d board[(row-1)*cols+(col-1)]==1) neighbors++; if (d board[(row-1)*cols+(col)] == 1) neighbors++; if (col!=(cols-1)) if (d board[(row-1)*cols+(col+1)]==1) neighbors++; if (col!=0) if (d board[(row)*cols+(col-1)]==1) neighbors++;

Computer Architecture Quantitative 5th Approach Solution Manual

Xiaolong Qi

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