

INTERNATIONAL EDITION

COMPUTER ORGANIZATION

fifth edition



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Zvonko Vranesic
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Computer Organization 5th Fifth Edition

Andrew Stuart Tanenbaum



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processor is overviewed to discuss what quantity we can use to measure the efficiency of these processors The proposed quantity is the ratio between the minimum possible energy consumption and the actual energy consumption for a given application using a given semiconductor technology In chapter 3 whether or not this quantity can be used in practice is discussed for many real world applications In chapter 4 general purpose processors in the past and present are discussed from this viewpoint In chapter 5 how we can actually design processors with near optimal efficiencies is described and in chapter 6 how we can program such processors This book gives a new way to look at the field of the design of high performance processors Computer Organization and Design MIPS Edition David A. Patterson, John L.

Hennessy, 2020-11-24 Computer Organization and Design The Hardware Software Interface Sixth Edition the leading award winning textbook from Patterson and Hennessy used by more than 40 000 students per year continues to present the most comprehensive and readable introduction to this core computer science topic Improvements to this new release include new sections in each chapter on Domain Specific Architectures DSA and updates on all real world examples that keep it fresh and relevant for a new generation of students Covers parallelism in depth with examples and content highlighting parallel hardware and software topics Includes new sections in each chapter on Domain Specific Architectures DSA Discusses and highlights the Eight Great Ideas of computer architecture including Performance via Parallelism Performance via Pipelining Performance via Prediction Design for Moore's Law Hierarchy of Memories Abstraction to Simplify Design Make the Common Case Fast and Dependability via Redundancy Itanium Architecture for Programmers James S. Evans, Gregory L. Trimper, 2003 Step by step guide to assembly language for the 64 bit Itanium processors with extensive examples Details of Explicitly Parallel Instruction Computing EPIC Instruction set addressing register stack engine predication I/O procedure calls floating point operations and more Learn how to comprehend and optimize open source Intel and HP UX compiler output Understand the full power of 64 bit Itanium EPIC processors Itaniumreg Architecture for Programmers is a comprehensive introduction to the breakthrough capabilities of the new 64 bit Itanium architecture Using standard command line tools and extensive examples the authors illuminate the Itanium design within the broader context of contemporary computer architecture via a step by step investigation of Itanium assembly language Coverage includes The potential of Explicitly Parallel Instruction Computing EPIC Itanium instruction formats and addressing modes Innovations such as the register stack engine RSE and extensive predication Procedure calls and procedure calling mechanisms Floating point operations I/O techniques from simple debugging to the use of files Optimization of output from open source Intel and HP UX compilers An essential resource for both computing professionals and students of architecture or assembly language Itanium Architecture for Programmers includes extensive printed and Web based references plus many numeric essay and programming exercises for each chapter *Structured Computer Organization 5th Ed* Andrew Stuart Tanenbaum, 2006

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