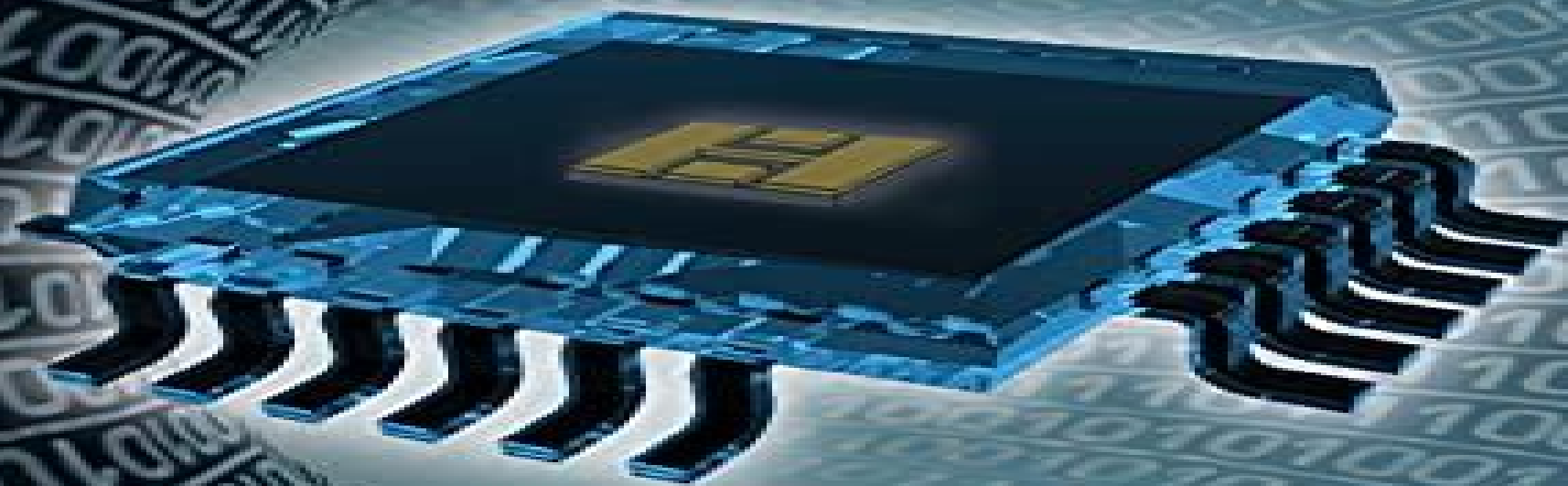


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Designing Network On-Chip Architectures in the Nanoscale Era



Edited by
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Designing Network On Chip Architectures In The Nanoscale Era Chapman Hallcrc Computational Science

**Jakub Kurzak, David A. Bader, Jack
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Designing Network On Chip Architectures In The Nanoscale Era Chapman Hallcrc Computational Science:

Designing Network On-Chip Architectures in the Nanoscale Era Jose Flich, Davide Bertozzi, 2010-12-18 Going beyond isolated research ideas and design experiences *Designing Network On Chip Architectures in the Nanoscale Era* covers the foundations and design methods of network on chip NoC technology The contributors draw on their own lessons learned to provide strong practical guidance on various design issues Exploring the design process of the *Network-on-Chip* Santanu Kundu, Santanu Chattopadhyay, 2018-09-03 Addresses the Challenges Associated with System on Chip Integration Network on Chip The Next Generation of System on Chip Integration examines the current issues restricting chip on chip communication efficiency and explores Network on chip NoC a promising alternative that equips designers with the capability to produce a scalable reusable and high performance communication backbone by allowing for the integration of a large number of cores on a single system on chip SoC This book provides a basic overview of topics associated with NoC based design communication infrastructure design communication methodology evaluation framework and mapping of applications onto NoC It details the design and evaluation of different proposed NoC structures low power techniques signal integrity and reliability issues application mapping testing and future trends Utilizing examples of chips that have been implemented in industry and academia this text presents the full architectural design of components verified through implementation in industrial CAD tools It describes NoC research and developments incorporates theoretical proofs strengthening the analysis procedures and includes algorithms used in NoC design and synthesis In addition it considers other upcoming NoC issues such as low power NoC design signal integrity issues NoC testing reconfiguration synthesis and 3 D NoC design This text comprises 12 chapters and covers The evolution of NoC from SoC its research and developmental challenges NoC protocols elaborating flow control available network topologies routing mechanisms fault tolerance quality of service support and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network on Chip The Next Generation of System on Chip Integration covers the basic topics technology and future trends relevant to NoC based design and can be used by engineers students and researchers and other industry professionals interested in computer architecture embedded systems and parallel distributed systems

Reliability, Availability and Serviceability of Networks-on-Chip Érika Cota, Alexandre de Moraes Amory, Marcelo Soares Lubaszewski, 2011-09-23 This book presents an overview of the issues related to the test diagnosis and fault tolerance of Network on Chip based systems It is the first book dedicated to the quality aspects of NoC based systems and will serve as an invaluable reference to the problems challenges solutions and trade offs related to designing and implementing state of the

art on chip communication architectures **Scientific Computing with Multicore and Accelerators** Jakub Kurzak, David A. Bader, Jack Dongarra, 2010-12-07 The hybrid heterogeneous nature of future microprocessors and large high performance computing systems will result in a reliance on two major types of components multicore manycore central processing units and special purpose hardware massively parallel accelerators While these technologies have numerous benefits they also pose substantial perfo *Application Analysis Tools for ASIP Design* Kingshuk Karuri, Rainer Leupers, 2011-06-15 This book introduces a novel design methodology which can significantly reduce the ASIP development effort through high degrees of design automation The key elements of this new design methodology are a powerful application profiler and an automated instruction set customization tool which considerably lighten the burden of mapping a target application to an ASIP architecture in the initial design stages The book includes several design case studies with real life embedded applications to demonstrate how the methodology and the tools can be used in practice for accelerating the overall ASIP design process

Future Control and Automation Wei Deng, 2012-06-26 This volume Future Control and Automation Volume 1 includes best papers selected from 2012 2nd International Conference on Future Control and Automation ICFA 2012 held on July 1 2 2012 Changsha China Future control and automation is the use of control systems and information technologies to reduce the need for human work in the production of goods and services This volume can be divided into five sessions on the basis of the classification of manuscripts considered which is listed as follows Identification and Control Navigation Guidance and Sensor Simulation Technology Future Telecommunications and Control *Сигнально-архитектурный реинжиниринг и радиосенсорное распознавание электронных средств* Михаил Костин, Константин Бойков, 2024-06-27 11 03 01 11 04 01 11 03 02 11 04 02 11 03 03 11 04 03 11 05 01 2 2 13 **Networks on Chips** Giovanni De Micheli, Luca Benini, 2006-08-30 The design of today s semiconductor chips for various applications such as telecommunications poses various challenges due to the complexity of these systems These highly complex systems on chips demand new approaches to connect and manage the communication between on chip processing and storage components and networks on chips NoCs provide a powerful solution This book is the first to provide a unified overview of NoC technology It includes in depth analysis of all the on chip communication challenges from physical wiring implementation up to software architecture and a complete classification of their various Network on Chip approaches and solutions Leading edge research from world renowned experts in academia and industry with state of the art technology implementations trends An integrated presentation not currently available in any other book A thorough introduction to current design methodologies and chips designed with NoCs

Networks on Chip Axel Jantsch, Hannu Tenhunen, 2007-05-08 As the number of processor cores and IP blocks integrated on a single chip is steadily growing a systematic approach to design the communication infrastructure becomes necessary Different variants of packed switched on chip networks have been proposed by several groups during the past two years This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to

architecture to operating systems and application interfaces It also provides a guideline and vision about the direction this field is moving to Moreover the book outlines the consequences of adopting design platforms based on packet switched network The consequences may in fact be far reaching because many of the topics of distributed systems distributed real time systems fault tolerant systems parallel computer architecture parallel programming as well as traditional system on chip issues will appear relevant but within the constraints of a single chip VLSI implementation **The Chip Is the Network**
Radu Marculescu,Paul Bogdan,2008-12-24 Addresses the concept of network in three different contexts representing the deterministic probabilistic and statistical physics inspired design paradigms

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