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### Chapter 2 Solutions

- 2.1 (a) VHDL - VHSIC Hardware Description Language  
VHSIC - Very High Speed Integrated Circuit
- (b) VHDL has statements that execute concurrently since it must model real hardware in which the components are all in operation at the same time.
- (c) A hardware description language allows a digital system to be designed and debugged at a higher level of abstraction than schematic capture with gates, flip-flops, and standard MSI building blocks. The details of the gates and flip-flops do not need to be handled during early phases of design. Designs are more portable when low-level library-specific details are not included in the model. HDLs allow the creation of such portable high-level behavioral models.

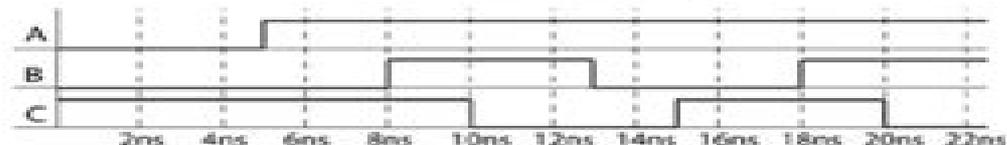
- 2.2 (a) Legal: A\_123, and1; Illegal: 123A (Starts with number), \_A123 (starts with underscore), A123\_ (ends with underscore), e1 e2 (adjacent underscores), and (reserved word).

(b) They all equivalent. VHDL is not case sensitive.

- 2.3 (a)



(b)



```
2.4 entity Comb is
  port(A, B, C, D : in bit;
        Z : out bit);
end Comb;
architecture Comb2_1 of Comb is
  signal E, F, G, H, I : bit;
begin
  H<=(A and B and C) after 5 ns;
  E<=H or D after 5 ns;
  G<=(B nor C) after 5 ns;
  F<=G nand A after 5 ns;
  I <= not F after 2 ns;
  Z<=E xor I after 5 ns;
end Comb2_1;
```

- 2.5 (a) entity one\_bit\_sub is  
port(x, y, bin: in bit;  
diff, bout: out bit);

# Digital Electronics With Vhdl Solution Manual

**Guillaume Favre**



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