

Bei Yu · David Z. Pan

Design for Manufacturability with Advanced Lithography

 Springer

Design For Manufacturability With Advanced Lithography

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Prinsloo**



Design For Manufacturability With Advanced Lithography:

Design for Manufacturability with Advanced Lithography Bei Yu, David Z. Pan, 2015-10-28 This book introduces readers to the most advanced research results on Design for Manufacturability DFM with multiple patterning lithography MPL and electron beam lithography EBL The authors describe in detail a set of algorithms methodologies to resolve issues in modern design for manufacturability problems with advanced lithography Unlike books that discuss DFM from the product level or physical manufacturing level this book describes DFM solutions from a circuit design level such that most of the critical problems can be formulated and solved through combinatorial algorithms

Design for Manufacturing with Advanced Lithography Bei Yu, 2014 Shrinking the feature size of very large scale integrated circuits VLSI with advanced lithography has been a holy grail for the semiconductor industry However the gap between manufacturing capability and the expectation of design performance becomes critically challenged in sub 16nm technology nodes To bridge this gap design for manufacturing DFM is a must to co optimize both design and lithography process at the same time DFM for advanced lithography could be defined very differently under different circumstances In general progress in advanced lithography happens along three different directions 1 New patterning technique e g layout decomposition for different patterning techniques 2 New design methodology e g lithography aware standard cell design and physical design 3 New illumination system e g layout fracturing for EBL system stencil planning for EBL system In this dissertation we present our research results on design for manufacturing DFM with multiple patterning lithography MPL and electron beam lithography EBL addressing these three DFM research directions in advanced lithography For the research direction of new patterning technique we study the layout decomposition problems for different patterning technique and explore four important topics 1 layout decomposition for triple patterning 2 density balanced layout decomposition for triple patterning 3 layout decomposition for triple patterning with end cutting 4 layout decomposition for quadruple patterning and beyond We present the proof that triple patterning layout decomposition is NP hard Besides we propose a number of CAD optimization and integration techniques to solve different problems For the research direction of new design methodology we will show the limitation of traditional design flow That is ignoring triple patterning lithography TPL in early stages may limit the potential to resolve all the TPL conflicts We propose a coherent framework including standard cell compliance and detailed placement to enable TPL friendly design Considering TPL constraints during early design stages such as standard cell compliance improves the layout decomposability With the pre coloring solutions of standard cells we present a TPL aware detailed placement where the layout decomposition and placement can be resolved simultaneously In addition we propose a linear dynamic programming to solve TPL aware detailed placement with maximum displacement which can achieve good trade off in terms of runtime and performance For the EBL illumination system we focus on two topics to improve the throughput of the whole EBL system 1 overlapping aware stencil planning under MCC system 2 L shape based layout fracturing for mask

preparation With simulations and experiments we demonstrate the critical role and effectiveness of DFM techniques for the advanced lithography as the semiconductor industry marches forward in the deeper sub micron domain **Design for**

Manufacturability and Statistical Design Michael Orshansky,Sani Nassif,Duane Boning,2007-10-28 Design for Manufacturability and Statistical Design A Constructive Approach provides a thorough treatment of the causes of variability methods for statistical data characterization and techniques for modeling analysis and optimization of integrated circuits to improve yield The objective of the constructive approach developed in this book is to formulate a consistent set of methods and principles necessary for rigorous statistical design and design for manufacturability from device physics to large scale circuit optimization The segments of the book are devoted respectively to understanding the causes of variability design of test structures for variability characterization statistically rigorous data analysis techniques of design for manufacturability in lithography and in chemical mechanical polishing statistical simulation analysis and optimization techniques for improving parametric yield Design for Manufacturability and Statistical Design A Constructive Approach presents an overview of the methods that need to be mastered for state of the art design for manufacturability and statistical design methodologies It is an important reference for practitioners and students in the field of computer aided design of integrated circuits **Design**

for Manufacturability Artur Balasinski,2013-10-05 This book explains integrated circuit design for manufacturability DfM at the product level packaging applications and applies engineering DfM principles to the latest standards of product development at 22 nm technology nodes It is a valuable guide for layout designers packaging engineers and quality engineers covering DfM development from 1D to 4D involving IC design flow setup best practices links to manufacturing and product definition for process technologies down to 22 nm node and product families including memories logic system on chip and system in package *Physical Design and Mask Synthesis for Directed Self-Assembly Lithography* Seongbo

Shim,Youngsoo Shin,2018-03-21 This book discusses physical design and mask synthesis of directed self assembly lithography DSAL It covers the basic background of DSAL technology physical design optimizations such as placement and redundant via insertion and DSAL mask synthesis as well as its verification Directed self assembly lithography DSAL is a highly promising patterning solution in sub 7nm technology SOC-Based Solutions in Emerging Application Domains

Veena S. Chakravarthi,Shivananda R. Koteswarar,2025-04-09 Working in the ever evolving field of smart chip design within an AI powered design environment the authors of this book draw on their experiences in successfully developing system on chip SoC solutions having grappled with the emerging design environment innovative tools domain specific challenges and major design decisions for SOC based solutions They present the first comprehensive guide to navigating the technical challenges of SOC based solutions in emerging application domains covering various design and development methodologies for system on chip solutions for emerging target applications When diligently applied the strategies and tactics presented can significantly shorten development timelines help avoid common pitfalls and improve the odds of success especially in AI

powered smart EDA environments The book provides a detailed insight into SoC based solutions for various applications including artificial intelligence AI post quantum security feature enhancements 3D SOC quantum SOC photonic SOC and SOC solutions for IoT high performance computing SOC and processor based systems The coverage includes architecture exploration methods for targeted applications compute intensive SoCs lightweight SoCs for IOT applications advanced technology node solutions and solutions including hardware software co designs and software defined SoCs The strategies best applied in these highly advanced technology developments are discussed in a guest chapter by a practicing high technology strategist so innovators designers entrepreneurs product managers investors and executives may properly prepare their companies to succeed

Nano-CMOS Design for Manufacturability Ban P. Wong, Anurag Mittal, Greg W. Starr, Franz Zach, Victor Moroz, Andrew Kahng, 2008-12-29 Discover innovative tools that pave the way from circuit and physical design to fabrication processing Nano CMOS Design for Manufacturability examines the challenges that design engineers face in the nano scaled era such as exacerbated effects and the proven design for manufacturability DFM methodology in the midst of increasing variability and design process interactions In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore's law the authors also tackle complex issues in the design process to overcome the difficulties including the use of a functional first silicon to support a predictable product ramp Moreover they introduce several emerging concepts including stress proximity effects contour based extraction and design process interactions This book is the sequel to Nano CMOS Circuit and Physical Design taking design to technology nodes beyond 65nm geometries It is divided into three parts Part One Newly Exacerbated Effects introduces the newly exacerbated effects that require designers attention beginning with a discussion of the lithography aspects of DFM followed by the impact of layout on transistor performance Part Two Design Solutions examines how to mitigate the impact of process effects discussing the methodology needed to make sub wavelength patterning technology work in manufacturing as well as design solutions to deal with signal power integrity WELL stress proximity effects and process variability Part Three The Road to DFM describes new tools needed to support DFM efforts including an auto correction tool capable of fixing the layout of cells with multiple optimization goals followed by a look ahead into the future of DFM Throughout the book real world examples simplify complex concepts helping readers see how they can successfully handle projects on Nano CMOS nodes It provides a bridge that allows engineers to go from physical and circuit design to fabrication processing and in short make designs that are not only functional but that also meet power and performance goals within the design schedule

Directed Self-assembly of Block Co-polymers for Nano-manufacturing Roel Gronheid, Paul Nealey, 2015-07-17 The directed self assembly DSA method of patterning for microelectronics uses polymer phase separation to generate features of less than 20nm with the positions of self assembling materials externally guided into the desired pattern Directed self assembly of Block Co polymers for Nano manufacturing reviews the design production applications and future developments

needed to facilitate the widescale adoption of this promising technology Beginning with a solid overview of the physics and chemistry of block copolymer BCP materials Part 1 covers the synthesis of new materials and new processing methods for DSA Part 2 then goes on to outline the key modelling and characterization principles of DSA reviewing templates and patterning using topographical and chemically modified surfaces line edge roughness and dimensional control x ray scattering for characterization and nanoscale driven assembly Finally Part 3 discusses application areas and related issues for DSA in nano manufacturing including for basic logic circuit design the inverse DSA problem design decomposition and the modelling and analysis of large scale template self assembly manufacturing techniques Authoritative outlining of theoretical principles and modeling techniques to give a thorough introduction to the topic Discusses a broad range of practical applications for directed self assembly in nano manufacturing Highlights the importance of this technology to both the present and future of nano manufacturing by exploring its potential use in a range of fields *VLSI and Chip Design* Dr. M. Maheswaran, Mandadupu Anusha, Bandam Narendar, Modugu Rambabu, 2024-05-23 VLSI and Chip Design exploration of Very Large Scale Integration VLSI technology and the intricacies of modern chip design It fundamental principles advanced methodologies and the latest innovations in circuit design fabrication and testing With a focus on digital and analog systems this integrates theoretical concepts with practical applications catering to both beginners and professionals It emphasizes design optimization power efficiency and scalability making it an essential resource for engineers researchers and students aspiring to excel in semiconductor technology and integrated circuit design Extending Moore's Law through Advanced Semiconductor Design and Processing Techniques Wynand Lambrechts, Saurabh Sinha, Jassem Ahmed Abdallah, Jaco Prinsloo, 2018-09-13 This book provides a methodological understanding of the theoretical and technical limitations to the longevity of Moore s law The book presents research on factors that have significant impact on the future of Moore s law and those factors believed to sustain the trend of the last five decades Research findings show that boundaries of Moore s law primarily include physical restrictions of scaling electronic components to levels beyond that of ordinary manufacturing principles and approaching the bounds of physics The research presented in this book provides essential background and knowledge to grasp the following principles Traditional and modern photolithography the primary limiting factor of Moore s law Innovations in semiconductor manufacturing that makes current generation CMOS processing possible Multi disciplinary technologies that could drive Moore s law forward significantly Design principles for microelectronic circuits and components that take advantage of technology miniaturization The semiconductor industry economic market trends and technical driving factors The complexity and cost associated with technology scaling have compelled researchers in the disciplines of engineering and physics to optimize previous generation nodes to improve system on chip performance This is especially relevant to participate in the increased attractiveness of the Internet of Things IoT This book additionally provides scholarly and practical examples of principles in microelectronic circuit design and layout to mitigate technology limits of

previous generation nodes Readers are encouraged to intellectually apply the knowledge derived from this book to further research and innovation in prolonging Moore s law and associated principles

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