

# DIGITAL SYSTEM CLOCKING

**High-Performance and Low-Power Aspects** 

VOJIN G. OKLOBOZIJA, VLADIMIR M. STOJANOVIC, DEJAN M. MARKOVIC, AND NIKOLA NEDOVIC

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# <u>Digital System Clocking High Performance And Low</u> <u>Power Aspects</u>

**Hubert Kaeslin** 

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synchronization and interconnect power supplies and switching noise low power circuits reconfigurable architectures circuits and methods power and delay modeling as well as power optimizations addressing reconfigurable architectures

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