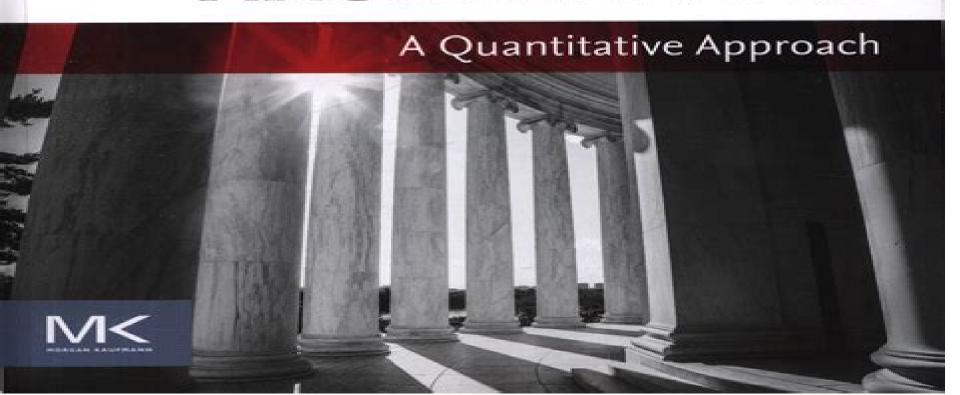
John L. Hennessy | David A. Patterson

# COMPUTER ARCHITECTURE



# **Computer Architecture A Quantitative Approach**

John L. Hennessy, David A. Patterson, Christos Kozyrakis

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Computer Architecture John L. Hennessy, David A. Patterson, 2002-05-29 This best selling title considered for over a decade to be essential reading for every serious student and practitioner of computer design has been updated throughout to address the most important trends facing computer designers today In this edition the authors bring their trademark method of quantitative analysis not only to high performance desktop machine design but also to the design of embedded and server systems They have illustrated their

principles with designs from all three of these domains including examples from consumer electronics multimedia and web technologies and high performance computing The book retains its highly rated features Fallacies and Pitfalls which share the hard won lessons of real designers Historical Perspectives which provide a deeper look at computer design history Putting it all Together which present a design example that illustrates the principles of the chapter Worked Examples which challenge the reader to apply the concepts theories and methods in smaller scale problems and Cross Cutting Issues which show how the ideas covered in one chapter interact with those presented in others In addition a new feature Another View presents brief design examples in one of the three domains other than the one chosen for Putting It All Together The authors present a new organization of the material as well reducing the overlap with their other text Computer Organization and Design A Hardware Software Approach 2 e and offering more in depth treatment of advanced topics in multithreading instruction level parallelism VLIW architectures memory hierarchies storage devices and network technologies Also new to this edition is the adoption of the MIPS 64 as the instruction set architecture In addition to several online appendixes two new appendixes will be printed in the book one contains a complete review of the basic concepts of pipelining the other provides solutions a selection of the exercises Both will be invaluable to the student or professional learning on her own or in the classroom Hennessy and Patterson continue to focus on fundamental techniques for designing real machines and for maximizing their cost performance Presents state of the art design examples including IA 64 architecture and its first implementation the Itanium Pipeline designs for Pentium III and Pentium IV The cluster that runs the Google search engine EMC storage systems and their performance Sony Playstation 2 Infiniband a new storage area and system area network SunFire 6800 multiprocessor server and its processor the UltraSPARC III Trimedia TM32 media processor and the Transmeta Crusoe processor Examines quantitative performance analysis in the commercial server market and the embedded market as well as the traditional desktop market Updates all the examples and figures with the most recent benchmarks such as SPEC 2000 Expands coverage of instruction sets to include descriptions of digital signal processors media processors and multimedia extensions to desktop processors Analyzes capacity cost and performance of disks over two decades Surveys the role of clusters in scientific computing and commercial computing Presents a survey taxonomy and the benchmarks of errors and failures in computer systems Presents detailed descriptions of the design of storage systems and of clusters Surveys memory hierarchies in modern microprocessors and the key parameters of modern disks Presents a glossary of networking terms **Computer Architecture** John L. Hennessy, David A. Patterson, 2006-11-03 The era of seemingly unlimited growth in processor performance is over single chip architectures can no longer overcome the performance limitations imposed by the power they consume and the heat they generate Today Intel and other semiconductor firms are abandoning the single fast processor model in favor of multi core microprocessors chips that combine two or more processors in a single package In the fourth edition of Computer Architecture the authors focus on this historic shift

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#### **Table of Contents Computer Architecture A Quantitative Approach**

- 1. Understanding the eBook Computer Architecture A Quantitative Approach
  - The Rise of Digital Reading Computer Architecture A Quantitative Approach
  - Advantages of eBooks Over Traditional Books
- 2. Identifying Computer Architecture A Quantitative Approach
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
- 3. Choosing the Right eBook Platform
  - $\circ \ \ Popular \ eBook \ Platforms$
  - Features to Look for in an Computer Architecture A Quantitative Approach
  - User-Friendly Interface
- 4. Exploring eBook Recommendations from Computer Architecture A Quantitative Approach
  - Personalized Recommendations

- Computer Architecture A Quantitative Approach User Reviews and Ratings
- Computer Architecture A Quantitative Approach and Bestseller Lists
- 5. Accessing Computer Architecture A Quantitative Approach Free and Paid eBooks
  - Computer Architecture A Quantitative Approach Public Domain eBooks
  - Computer Architecture A Quantitative Approach eBook Subscription Services
  - Computer Architecture A Quantitative Approach Budget-Friendly Options
- 6. Navigating Computer Architecture A Quantitative Approach eBook Formats
  - o ePub, PDF, MOBI, and More
  - Computer Architecture A Quantitative Approach Compatibility with Devices
  - Computer Architecture A Quantitative Approach Enhanced eBook Features
- 7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Computer Architecture A Quantitative Approach
  - Highlighting and Note-Taking Computer Architecture A Quantitative Approach
  - Interactive Elements Computer Architecture A Quantitative Approach
- 8. Staying Engaged with Computer Architecture A Quantitative Approach
  - o Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers Computer Architecture A Quantitative Approach
- 9. Balancing eBooks and Physical Books Computer Architecture A Quantitative Approach
  - ∘ Benefits of a Digital Library
  - Creating a Diverse Reading Collection Computer Architecture A Quantitative Approach
- 10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
- 11. Cultivating a Reading Routine Computer Architecture A Quantitative Approach
  - Setting Reading Goals Computer Architecture A Quantitative Approach
  - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Computer Architecture A Quantitative Approach
  - Fact-Checking eBook Content of Computer Architecture A Quantitative Approach

- Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
  - Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
- 14. Embracing eBook Trends
  - Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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