



Short channel Effects in Deep Submicron CMOS

Computational Scaling Technology For Deep Submicron Design

LP Steffe



Computational Scaling Technology For Deep Submicron Design:

Computational Scaling Technology for Deep Submicron Design Kafai Lai, 2015-09-15 An understanding of computational scaling technology CST is essential for researchers and professionals involved in semiconductor design The first book to thoroughly explain CST this work provides ideas and directions for fully integrating design and technology within the field Focusing on modeling and simulations in computational lithography and design constraint optimization the book discusses the latest developments in design for manufacturing along with related design methods and challenges Examples of real world design technology co optimization DTCO test cases will help readers master the technology Proceedings of the Second International Conference on Computational Intelligence and Informatics Vikrant Bhateja, João Manuel R.S. Tavares, B. Padmaja Rani, V. Kamakshi Prasad, K. Srujan Raju, 2018-07-23 The volume contains 69 high quality papers presented at International Conference on Computational Intelligence and Informatics ICCII 2017 The conference was held during 25 27 September 2017 at Department of Computer Science and Engineering JNTUHCEH Hyderabad Telangana India This volume contains papers mainly focused on data mining wireless sensor networks parallel computing image processing network security MANETS natural language processing and internet of things Low Power Design in Deep Submicron Electronics W. Nebel, Jean Mermet, 2013-06-29 Low Power Design in Deep Submicron Electronics deals with the different aspects of low power design for deep submicron electronics at all levels of abstraction from system level to circuit level and technology Its objective is to guide industrial and academic engineers and researchers in the selection of methods technologies and tools and to provide a baseline for further developments Furthermore the book has been written to serve as a textbook for postgraduate student courses In order to achieve both goals it is structured into different chapters each of which addresses a different phase of the design a particular level of abstraction a unique design style or technology These design related chapters are amended by motivations in Chapter 2 which presents visions both of future low power applications and technology advancements and by some advanced case studies in Chapter 9 From the Foreword This global nature of design for low power was well understood by Wolfgang Nebel and Jean Mermet when organizing the NATO workshop which is the origin of the book They invited the best experts in the field to cover all aspects of low power design As a result the chapters in this book are covering deep submicron CMOS digital system design for low power in a systematic way from process technology all the way up to software design and embedded software systems Low Power Design in Deep Submicron Electronics is an excellent guide for the practicing engineer the researcher and the student interested in this crucial aspect of actual CMOS design It contains about a thousand references to all aspects of the recent five years of feverish activity in this exciting aspect of design Hugo de Man Professor K U Leuven Belgium Senior Research Fellow IMEC Belgium VLSI and Chip Design Dr. M. Maheswaran, Mandadupu Anusha, Bandam Narendar, Modugu Rambabu, 2024-05-23 VLSI and Chip Design exploration of Very Large Scale Integration VLSI technology and the intricacies of modern chip design It fundamental

principles advanced methodologies and the latest innovations in circuit design fabrication and testing With a focus on digital and analog systems this integrates theoretical concepts with practical applications catering to both beginners and professionals It emphasizes design optimization power efficiency and scalability making it an essential resource for engineers researchers and students aspiring to excel in semiconductor technology and integrated circuit design

Networks on Chip Axel Jantsch,Hannu Tenhunen,2007-05-08 As the number of processor cores and IP blocks integrated on a single chip is steadily growing a systematic approach to design the communication infrastructure becomes necessary Different variants of packed switched on chip networks have been proposed by several groups during the past two years This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces It also provides a guideline and vision about the direction this field is moving to Moreover the book outlines the consequences of adopting design platforms based on packet switched network The consequences may in fact be far reaching because many of the topics of distributed systems distributed real time systems fault tolerant systems parallel computer architecture parallel programming as well as traditional system on chip issues will appear relevant but within the constraints of a single chip VLSI implementation

Energy Systems Design for Low-Power Computing Gatti, Rathishchandra Ramachandra,Singh, Chandra,P., Srividya,Bhat, Sandeep,2023-03-07 With the advancement in computing technologies the need for power is also increasing Approximately 3% of the total power consumption is spent by data centers and computing devices This percentage will rise when more internet of things IoT devices are connected to the web The handling of this data requires immense power Energy Systems Design for Low Power Computing disseminates the current research and the state of the art technologies topologies standards and techniques for the deployment of energy intelligence in edge computing distributed computing and centralized computing infrastructure Covering topics such as electronic cooling stochastic data analysis and energy consumption this premier reference source is an excellent resource for data center designers VLSI designers network developers students and teachers of higher education librarians researchers and academicians

Photonic Interconnects for Computing Systems Gabriela Nicolescu,Mahdi Nikdast,Sébastien Le Beux,2022-09-01 In recent years there has been a considerable amount of effort both in industry and academia focusing on the design implementation performance analysis evaluation and prediction of silicon photonic interconnects for inter and intra chip communication paving the way for the design and dimensioning of the next and future generation of high performance computing systems Photonic Interconnects for Computing Systems provides a comprehensive overview of the current state of the art technology and research achievements in employing silicon photonics for interconnection networks and high performance computing summarizing main opportunities and some challenges The majority of the chapters were collected from presentations made at the International Workshop on Optical Photonic Interconnects for Computing Systems OPTICS held over the past two years The workshop invites internationally recognized speakers on the range of topics

relevant to silicon photonics and computing systems Technical topics discussed in the book include Design and Implementation of Chip Scale Photonic Interconnects Developing Design Automation Solutions for Chip Scale Photonic Interconnects Design Space Exploration in Chip Scale Photonic Interconnects Thermal Analysis and Modeling in Photonic Interconnects Design for Reliability Fabrication Non Uniformity in Photonic Interconnects Photonic Interconnects for Computing Systems presents a compilation of outstanding contributions from leading research groups in the field It presents a comprehensive overview of the design advantages challenges and requirements of photonic interconnects for computing systems The selected contributions present important discussions and approaches related to the design and development of novel photonic interconnect architectures as well as various design solutions to improve the performance of such systems while considering different challenges The book is ideal for personnel in computer photonic industries as well as academic staff and master graduate students in computer science and engineering electronic engineering electrical engineering and photonics

Computational Intelligence in Digital and Network Designs and Applications Mourad Fakhfakh, Esteban Tlelo-Cuautle, Patrick Siarry, 2015-07-14 This book explains the application of recent advances in computational intelligence algorithms design methodologies and synthesis techniques to the design of integrated circuits and systems It highlights new biasing and sizing approaches and optimization techniques and their application to the design of high performance digital VLSI radio frequency and mixed signal circuits and systems This second of two related volumes addresses digital and network designs and applications with 12 chapters grouped into parts on digital circuit design network optimization and applications It will be of interest to practitioners and researchers in computer science and electronics engineering engaged with the design of electronic circuits

Design and Test Strategies for 2D/3D Integration for NoC-based Multicore Architectures Kanchan Manna, Jimson Mathew, 2019-12-20 This book covers various aspects of optimization in design and testing of Network on Chip NoC based multicore systems It gives a complete account of the state of the art and emerging techniques for near optimal mapping and test scheduling for NoC based multicores The authors describe the use of the Integer Linear Programming ILP technique for smaller benchmarks and a Particle Swarm Optimization PSO to get a near optimal mapping and test schedule for bigger benchmarks The PSO based approach is also augmented with several innovative techniques to get the best possible solution The tradeoff between performance communication or test time of the system and thermal safety is also discussed based on designer specifications Provides a single source reference to design and test for circuit and system level approaches to NoC based multicore systems Gives a complete account of the state of the art and emerging techniques for near optimal mapping and test scheduling in NoC based multicore systems Organizes chapters systematically and hierarchically rather than in an ad hoc manner covering aspects of optimization in design and testing of Network on Chip NoC based multicore systems

High Performance Computing for Big Data Chao Wang, 2017-10-16 High Performance Computing for Big Data Methodologies and Applications explores emerging high performance

architectures for data intensive applications novel efficient analytical strategies to boost data processing and cutting edge applications in diverse fields such as machine learning life science neural networks and neuromorphic engineering The book is organized into two main sections The first section covers Big Data architectures including cloud computing systems and heterogeneous accelerators It also covers emerging 3D IC design principles for memory architectures and devices The second section of the book illustrates emerging and practical applications of Big Data across several domains including bioinformatics deep learning and neuromorphic engineering Features Covers a wide range of Big Data architectures including distributed systems like Hadoop Spark Includes accelerator based approaches for big data applications such as GPU based acceleration techniques and hardware acceleration such as FPGA CGRA ASICs Presents emerging memory architectures and devices such as NVM STT RAM 3D IC design principles Describes advanced algorithms for different big data application domains Illustrates novel analytics techniques for Big Data applications scheduling mapping and partitioning methodologies Featuring contributions from leading experts this book presents state of the art research on the methodologies and applications of high performance computing for big data applications About the Editor Dr Chao Wang is an Associate Professor in the School of Computer Science at the University of Science and Technology of China He is the Associate Editor of ACM Transactions on Design Automations for Electronics Systems TODAES Applied Soft Computing Microprocessors and Microsystems IET Computers Digital Techniques and International Journal of Electronics Dr Chao Wang was the recipient of Youth Innovation Promotion Association CAS ACM China Rising Star Honorable Mention 2016 and best IP nomination of DATE 2015 He is now on the CCF Technical Committee on Computer Architecture CCF Task Force on Formal Methods He is a Senior Member of IEEE Senior Member of CCF and a Senior Member of ACM

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