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Architectures for Computer Vision Hong Jeong, 2014-08-05 This book provides comprehensive coverage of 3D vision systems from vision models and state of the art algorithms to their hardware architectures for implementation on DSPs FPGA and ASIC chips and GPUs It aims to fill the gaps between computer vision algorithms and real time digital circuit implementations especially with Verilog HDL design The organization of this book is vision and hardware module directed based on Verilog vision modules 3D vision modules parallel vision architectures and Verilog designs for the stereo matching system with various parallel architectures Provides Verilog vision simulators tailored to the design and testing of general vision chips Bridges the differences between C C and HDL to encompass both software realization and chip implementation includes numerous examples that realize vision algorithms and general vision processing in HDL Unique in providing an organized and complete overview of how a real time 3D vision system on chip can be designed Focuses on the digital VLSI aspects and implementation of digital signal processing tasks on hardware platforms such as ASICs and FPGAs for 3D vision systems which have not been comprehensively covered in one single book Provides a timely view of the pervasive use of vision systems and the challenges of fusing information from different vision modules Accompanying website includes software and HDL code packages to enhance further learning and develop advanced systems A solution set and lecture slides are provided on the book s companion website The book is aimed at graduate students and researchers in computer vision and embedded systems as well as chip and FPGA designers Senior undergraduate students specializing in VLSI design or computer vision will also find the book to be helpful in understanding advanced applications

An Event-Driven Parallel-Processing Subsystem for Energy-Efficient Mobile Medical Instrumentation Florian Stefan Glaser, 2022-12-02 Aging population and the thereby ever rising cost of health services call for novel and innovative solutions for providing medical care and services So far medical care is primarily provided in the form of time consuming in person appointments with trained personnel and expensive stationary instrumentation equipment As for many current and past challenges the advances in microelectronics are a crucial enabler and offer a plethora of opportunities With key building blocks such as sensing processing and communication systems and circuits getting smaller cheaper and more energy efficient personal and wearable or even implantable point of care devices with medicalgrade instrumentation capabilities become feasible Device size and battery lifetime are paramount for the realization of such devices Besides integrating the required functionality into as few individual microelectronic components as possible the energy efficiency of such is crucial to reduce battery size

usually being the dominant contributor to overall device size In this thesis we present two major contributions to achieve the discussed goals in the context of miniaturized medical instrumentation First we present a synchronization solution for embedded parallel near threshold computing NTC a promising concept for enabling the required processing capabilities with an energy efficiency that is suitable for highly mobile devices with very limited battery capacity Our proposed solution aims at increasing energy efficiency and performance for parallel NTC clusters by maximizing the effective utilization of the available cores under parallel workloads We describe a hardware unit that enables fine grain parallelization by greatly optimizing and accelerating core to core synchronization and communication and analyze the impact of those mechanisms on the overall performance and energy efficiency of an eight core cluster With a range of digital signal processing DSP applications typical for the targeted systems the proposed hardware unit improves performance by up to 92% and 23% on average and energy efficiency by up to 98% and 39% on average In the second part we present a MCU processing and control subsystem MPCS for the integration into VivoSoC a highly versatile single chip solution for mobile medical instrumentation In addition to the MPCS it includes a multitude of analog front ends AFEs and a multi channel power management IC PMIC for voltage conversion

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