

Chapter 3 SOLUTIONS

1) a) $I_D = \frac{V_{in} - 2V_{D0n}}{R_1 + R_2}$

$$= \frac{2.5 - 1.4}{4k\Omega} = \frac{1.1V}{4k\Omega}$$

$$I_D = 275\mu A$$

b) $I_S = 10^{-14} A$, $T = 300K$, $V_{D0n} = 0.7V$

$$I_D = I_S (e^{V_D/\phi_T} - 1)$$

where $\phi_T = \frac{kT}{q} = 26mV @ 300K$

⊛ $I_D = \frac{V_{in} - 2V_D}{R_1 + R_2} = I_S (e^{V_D/\phi_T} - 1)$
 $\frac{2.5 - 2V_D}{4k\Omega} = 10^{-14} (e^{V_D/0.026} - 1)$

iterating on this expression
we can obtain.

$$V_D = 0.628V$$

$$I_D = 311\mu A$$

c) SPICE

exercise 3.1

```
vin in 0 dc 2.5
r1 in 2 2k
d1 2 3 D
r2 3 out 2k
d2 out 0 D
```

```
.options post=2
.op
```

```
.model D D level=1 is=1e-14 n=0.5
```

```
.end
```

```
*****
NODE      VOLTAGE
2         1.8750E+00
3         1.2500E+00
OUT       6.2501E-01
```

CURRENT 3.1249E-04

d) $I_S = 10^{-14} A$, $T = 300K$;
again use ⊛ from b and iterate
to find:

$$V_D = 0.743V$$

$$I_D = 253\mu A$$

$I_S = 10^{-14} A$, $T = 350K$;

$$V_D = 0.728V$$

$$I_D = 261\mu A$$

```
exercise 3.1d
vin in 0 dc 2.5
r1 in 2 2k
d1 2 3 D
r2 3 out 2k
d2 out 0 D
```

```
.options post=2
.op
```

```
*.temp 27
*.temp 77
*.model D D level=1 is=1e-14 n=0.5
*.model D D level=1 is=1e-14 n=0.5
.end
```

```
*****
t=27C*
NODE      VOLTAGE
2         1.9890E+00
3         1.2500E+00
IN        2.5000E+00
OUT       7.3892E-01
```

```
ID        2.5554E-04
*****
t=77C*
NODE      VOLTAGE
2         1.7844E+00
3         1.2500E+00
IN        2.5000E+00
OUT       5.3436E-01
```

ID 3.5782E-04

Digital Integrated Circuits Second Edition Solution Manual

Karin Nielsen-Saines



Digital Integrated Circuits Second Edition Solution Manual:

Solutions Manual Digital Integrated Circuits CRC Press, 2009-07-10 Any textbook more than five years old simply won't do in digital integrated circuits as dynamic CMOS circuits have emerged to dominate the field. Providing a revised instructional text for engineers involved with Very Large Scale Integrated Circuit design and fabrication, this second edition delves into the dramatic advances including new applications and changes in the physics of operation made possible by relentless miniaturization. Each chapter includes numerous worked examples, case studies, and SPICE computer simulations. The book's website offers supplementary material and more worked problems. Qualifying instructors will have access to a new instructor's manual. *Solution Manual to Accompany CMOS Digital Integrated Circuits : Analysis and Design, Second Edition* Sung-Mo Kang, Yusuf Leblebici, 1999

Embedded SoPC Design with Nios II Processor and Verilog Examples Pong P. Chu, 2012-05-14 Explores the unique hardware programmability of FPGA-based embedded systems using a learn-by-doing approach to introduce the concepts and techniques for embedded SoPC design with Verilog. An SoPC system on a programmable chip integrates a processor, memory, modules, I/O peripherals, and custom hardware accelerators into a single FPGA field-programmable gate array device. In addition to the customized software, customized hardware can be developed and incorporated into the embedded system as well, allowing us to configure the soft-core processor, create tailored I/O interfaces, and develop specialized hardware accelerators for computation-intensive tasks. Utilizing an Altera FPGA prototyping board and its Nios II soft-core processor, *Embedded SoPC Design with Nios II Processor and Verilog Examples* takes a learn-by-doing approach to illustrate the hardware and software design and development process by including realistic projects that can be implemented and tested on the board. Emphasizing hardware design and integration throughout, the book is divided into four major parts. Part I covers HDL and synthesis of custom hardware. Part II introduces the Nios II processor and provides an overview of embedded software development. Part III demonstrates the design and development of hardware and software of several complex I/O peripherals, including a PS2 keyboard and mouse, a graphic video controller, an audio codec, and an SD secure digital card. Part IV provides several case studies of the integration of hardware accelerators, including a custom GCD (greatest common divisor) circuit, a Mandelbrot set fractal circuit, and an audio synthesizer based on DDFS (direct digital frequency synthesis) methodology. While designing and developing an embedded SoPC can be rewarding, the learning can be a long and winding journey. This book shows the trail ahead and guides readers through the initial steps to exploit the full potential of this emerging methodology. **Embedded SoPC Design with Nios II Processor and VHDL Examples**

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