

Lieven Eeckhout

Computer Architecture Performance Evaluation Methods

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Evaluation Methods

Lieven Eeckhout



Computer Architecture Performance Evaluation Methods Computer Architecture Performance Evaluation Methods:

Computer Architecture Performance Evaluation Methods Lieven Eeckhout, 2022-05-31 Performance evaluation is at the foundation of computer architecture research and development Contemporary microprocessors are so complex that architects cannot design systems based on intuition and simple models only Adequate performance evaluation methods are absolutely crucial to steer the research and development process in the right direction However rigorous performance evaluation is non trivial as there are multiple aspects to performance evaluation such as picking workloads selecting an appropriate modeling or simulation approach running the model and interpreting the results using meaningful metrics Each of these aspects is equally important and a performance evaluation method that lacks rigor in any of these crucial aspects may lead to inaccurate performance data and may drive research and development in a wrong direction The goal of this book is to present an overview of the current state of the art in computer architecture performance evaluation with a special emphasis on methods for exploring processor architectures The book focuses on fundamental concepts and ideas for obtaining accurate performance data The book covers various topics in performance evaluation ranging from performance metrics to workload selection to various modeling approaches including mechanistic and empirical modeling And because simulation is by far the most prevalent modeling technique more than half the book s content is devoted to simulation The book provides an overview of the simulation techniques in the computer designer s toolbox followed by various simulation acceleration techniques including sampled simulation statistical simulation parallel simulation and hardware accelerated simulation Table of Contents Introduction Performance Metrics Workload Design Analytical Performance Modeling Simulation Sampled Simulation Statistical Simulation Parallel Simulation and Hardware Acceleration Concluding Remarks

Computer Performance Measurement and Evaluation Methods Liba Svobodova, 1976 Performance evaluation is not just determining whether or not a system meets certain objectives it is also understanding if and how system performance can be improved A computer system analyst must master a number of techniques to ascertain important factors and their effect on system performance The purpose of this book is to develop a better understanding of the problem of performance evaluation and to analyze available techniques within this concept Directed to present and future computer analysts and designers readers should be familiar with concepts of hardware organization system architecture and operating systems

Synthesis Lectures on Computer Architecture : Computer Architecture Performance Evaluation Methods Lieven Eeckhout, *A Primer on Memory Consistency and Cache Coherence, Second Edition* Vijay Nagarajan, Daniel J. Sorin, Mark D. Hill, David A. Wood, 2022-05-31 Many modern computer systems including homogeneous and heterogeneous architectures support shared memory in hardware In a shared memory system each of the processor cores may read and write to a single shared address space For a shared memory machine the memory consistency model defines the

architecturally visible behavior of its memory system Consistency definitions provide rules about loads and stores or memory reads and writes and how they act upon memory As part of supporting a memory consistency model many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up to date The goal of this primer is to provide readers with a basic understanding of consistency and coherence This understanding includes both the issues that must be solved as well as a variety of solutions We present both high level concepts as well as specific concrete examples from real world systems This second edition reflects a decade of advancements since the first edition and includes among other more modest changes two new chapters one on consistency and coherence for non CPU accelerators with a focus on GPUs and one that points to formal work and tools on consistency and coherence

On-Chip Networks Natalie Enright Jerger, Tushar Krishna, Li-Shiuan Peh, 2017-06-19 This book targets engineers and researchers familiar with basic computer architecture concepts who are interested in learning about on chip networks This work is designed to be a short synthesis of the most critical concepts in on chip network design It is a resource for both understanding on chip network basics and for providing an overview of state of the art research in on chip networks We believe that an overview that teaches both fundamental concepts and highlights state of the art designs will be of great value to both graduate students and industry engineers While not an exhaustive text we hope to illuminate fundamental concepts for the reader as well as identify trends and gaps in on chip network research With the rapid advances in this field we felt it was timely to update and review the state of the art in this second edition We introduce two new chapters at the end of the book We have updated the latest research of the past years throughout the book and also expanded our coverage of fundamental concepts to include several research ideas that have now made their way into products and in our opinion should be textbook concepts that all on chip network practitioners should know For example these fundamental concepts include message passing multicast routing and bubble flow control schemes

On-Chip Networks, Second Edition Natalie Enright Jerger, Tushar Krishna, Li-Shiuan Peh, 2022-05-31 This book targets engineers and researchers familiar with basic computer architecture concepts who are interested in learning about on chip networks This work is designed to be a short synthesis of the most critical concepts in on chip network design It is a resource for both understanding on chip network basics and for providing an overview of state of the art research in on chip networks We believe that an overview that teaches both fundamental concepts and highlights state of the art designs will be of great value to both graduate students and industry engineers While not an exhaustive text we hope to illuminate fundamental concepts for the reader as well as identify trends and gaps in on chip network research With the rapid advances in this field we felt it was timely to update and review the state of the art in this second edition We introduce two new chapters at the end of the book We have updated the latest research of the past years throughout the book and also expanded our coverage of fundamental concepts to include several research ideas that have now made their way into products and in our opinion should be textbook concepts that all on chip network practitioners should know For

example these fundamental concepts include message passing multicast routing and bubble flow control schemes

Phase Change Memory Naveen Muralimanohar, Moinuddin K. Qureshi, Sudhanva Gurumurthi, Bipin Rajendran, 2022-05-31 As conventional memory technologies such as DRAM and Flash run into scaling challenges architects and system designers are forced to look at alternative technologies for building future computer systems This synthesis lecture begins by listing the requirements for a next generation memory technology and briefly surveys the landscape of novel non volatile memories Among these Phase Change Memory PCM is emerging as a leading contender and the authors discuss the material device and circuit advances underlying this exciting technology The lecture then describes architectural solutions to enable PCM for main memories Finally the authors explore the impact of such byte addressable non volatile memories on future storage and system designs Table of Contents Next Generation Memory Technologies Architecting PCM for Main Memories Tolerating Slow Writes in PCM Wear Leveling for Durability Wear Leveling Under Adversarial Settings Error Resilience in Phase Change Memories Storage and System Design With Emerging Non Volatile Memories *A Primer on Hardware Prefetching* Babak Falsafi, Thomas F. Wenisch, 2022-06-01 Since the 1970 s microprocessor based digital platforms have been riding Moore s law allowing for doubling of density for the same area roughly every two years However whereas microprocessor fabrication has focused on increasing instruction execution rate memory fabrication technologies have focused primarily on an increase in capacity with negligible increase in speed This divergent trend in performance between the processors and memory has led to a phenomenon referred to as the Memory Wall To overcome the memory wall designers have resorted to a hierarchy of cache memory levels which rely on the principal of memory access locality to reduce the observed memory access time and the performance gap between processors and memory Unfortunately important workload classes exhibit adverse memory access patterns that baffle the simple policies built into modern cache hierarchies to move instructions and data across cache levels As such processors often spend much time idling upon a demand fetch of memory blocks that miss in higher cache levels Prefetching predicting future memory accesses and issuing requests for the corresponding memory blocks in advance of explicit accesses is an effective approach to hide memory access latency There have been a myriad of proposed prefetching techniques and nearly every modern processor includes some hardware prefetching mechanisms targeting simple and regular memory access patterns This primer offers an overview of the various classes of hardware prefetchers for instructions and data proposed in the research literature and presents examples of techniques incorporated into modern microprocessors

Multi-Core Cache Hierarchies Rajeev Balasubramonian, Norman Paul Jouppi, Naveen Muralimanohar, 2011 A key determinant of overall system performance and power dissipation is the cache hierarchy since access to off chip memory consumes many more cycles and energy than on chip accesses In addition multi core processors are expected to place ever higher bandwidth demands on the memory system All these issues make it important to avoid off chip memory access by improving the efficiency of the on chip cache Future multi core processors will have many large

cache banks connected by a network and shared by many cores Hence many important problems must be solved cache resources must be allocated across many cores data must be placed in cache banks that are near the accessing core and the most important data must be identified for retention Finally difficulties in scaling existing technologies require adapting to and exploiting new technology constraints The book attempts a synthesis of recent cache research that has focused on innovations for multi core processors It is an excellent starting point for early stage graduate students researchers and practitioners who wish to understand the landscape of recent cache research The book is suitable as a reference for advanced computer architecture classes as well as for experienced researchers and VLSI engineers Table of Contents Basic Elements of Large Cache Design Organizing Data in CMP Last Level Caches Policies Impacting Cache Hit Rates Interconnection Networks within Large Caches Technology Concluding Remarks

Space-Time Computing with Temporal Neural Networks James E. Smith, 2022-05-31 Understanding and implementing the brain's computational paradigm is the one true grand challenge facing computer researchers Not only are the brain's computational capabilities far beyond those of conventional computers its energy efficiency is truly remarkable This book written from the perspective of a computer designer and targeted at computer researchers is intended to give both background and lay out a course of action for studying the brain's computational paradigm It contains a mix of concepts and ideas drawn from computational neuroscience combined with those of the author As background relevant biological features are described in terms of their computational and communication properties The brain's neocortex is constructed of massively interconnected neurons that compute and communicate via voltage spikes and a strong argument can be made that precise spike timing is an essential element of the paradigm Drawing from the biological features a mathematics based computational paradigm is constructed The key feature is spiking neurons that perform communication and processing in space time with emphasis on time In these paradigms time is used as a freely available resource for both communication and computation Neuron models are first discussed in general and one is chosen for detailed development Using the model single neuron computation is first explored Neuron inputs are encoded as spike patterns and the neuron is trained to identify input pattern similarities Individual neurons are building blocks for constructing larger ensembles referred to as columns These columns are trained in an unsupervised manner and operate collectively to perform the basic cognitive function of pattern clustering Similar input patterns are mapped to a much smaller set of similar output patterns thereby dividing the input patterns into identifiable clusters Larger cognitive systems are formed by combining columns into a hierarchical architecture These higher level architectures are the subject of ongoing study and progress to date is described in detail in later chapters Simulation plays a major role in model development and the simulation infrastructure developed by the author is described

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