

DIGITAL SYSTEMS TESTING AND TESTABLE DESIGN

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Digital Systems Testing Testable Design

**Laung-Terng Wang, Cheng-Wen
Wu, Xiaoqing Wen**



Digital Systems Testing Testable Design:

Digital Systems Testing and Testable Design Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman, 1990-01-01 A textbook in digital system testing and testable design Incorporating a significant amount of new material related to recently developed technologies this book offers comprehensive and state of the art treatment of both testing and testable design

Digital System Test and Testable Design Zainalabedin Navabi, 2010-12-10 This book is about digital system testing and testable design The concepts of testing and testability are treated together with digital design practices and methodologies The book uses Verilog models and testbenches for implementing and explaining fault simulation and test generation algorithms Extensive use of Verilog and Verilog PLI for test applications is what distinguishes this book from other test and testability books Verilog eliminates ambiguities in test algorithms and BIST and DFT hardware architectures and it clearly describes the architecture of the testability hardware and its test sessions Describing many of the on chip decompression algorithms in Verilog helps to evaluate these algorithms in terms of hardware overhead and timing and thus feasibility of using them for System on Chip designs Extensive use of testbenches and testbench development techniques is another unique feature of this book Using PLI in developing testbenches and virtual testers provides a powerful programming tool interfaced with hardware described in Verilog This mixed hardware software environment facilitates description of complex test programs and test strategies

Digital Systems Testing And Testable Design Miron Abramovici, 2001 This textbook provides a comprehensive and detailed treatment of digital systems testing and testable design It covers thoroughly both the fundamental concepts and the latest advances in this rapidly changing field and presents only theoretical material that supports practical applications Successfully used worldwide this book is an invaluable tool for test engineers ASIC and system designers and CAD developers

VLSI Test Principles and Architectures

Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, 2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures

Design of Systems on a Chip: Design and Test

Ricardo Reis, Marcelo Soares Lubaszewski, Jochen A.G. Jess, 2007-05-06 This book is the second of two volumes addressing the design challenges associated with new generations of semiconductor technology The various chapters are compiled from tutorials presented at workshops in recent years by prominent authors from all over the world Technology productivity and quality are the main aspects under consideration to establish the major requirements for the design and test of upcoming systems on a chip

Principles of Testing Electronic Systems Samiha Mourad, Yervant Zorian, 2000-07-25 A pragmatic approach to testing electronic systems As we move ahead in the electronic age rapid changes in technology pose an ever

increasing number of challenges in testing electronic products Many practicing engineers are involved in this arena but few have a chance to study the field in a systematic way learning takes place on the job By covering the fundamental disciplines in detail Principles of Testing Electronic Systems provides design engineers with the much needed knowledge base Divided into five major parts this highly useful reference relates design and tests to the development of reliable electronic products shows the main vehicles for design verification examines designs that facilitate testing and investigates how testing is applied to random logic memories FPGAs and microprocessors Finally the last part offers coverage of advanced test solutions for today s very deep submicron designs The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail Special features include An explanation of where a test belongs in the design flow Detailed discussion of scan path and ordering of scan chains BIST solutions for embedded logic and memory blocks Test methodologies for FPGAs A chapter on testing system on a chip Numerous references

Reliability Engineering Alessandro Birolini, 2003-08-20 Using clear language this book shows you how to build in evaluate and demonstrate reliability and availability of components equipment and systems It presents the state of the art in theory and practice and is based on the author s 30 years experience half in industry and half as professor of reliability engineering at the ETH Zurich In this extended edition new models and considerations have been added for reliability data analysis and fault tolerant reconfigurable repairable systems including reward and frequency duration aspects New design rules for imperfect switching incomplete coverage items with more than 2 states and phased mission systems as well as a Monte Carlo approach useful for rare events are given Trends in quality management are outlined Methods and tools are given in such a way that they can be tailored to cover different reliability requirement levels and be used to investigate safety as well The book contains a large number of tables figures and examples to support the practical aspects

The Small Book About Design-for-Test Juergen Alt, 2025-05-30 This book is designed for individuals working in the semiconductor industry who need a fundamental understanding of Design for Test DfT methods It caters to test and product engineers who typically utilize these methods as well as chip designers project managers and business owners who seek to comprehend the value of implemented DfT methods Additionally it serves as a starting point for beginners in DfT before delving deeper into implementation tools and test pattern generation tasks Originating from a university lecture the core content of this book has expanded over the years It bridges the gap between theoretical textbook descriptions of DfT and its practical application in the industry The goal is to present DfT as a collection of methods that maintain manufacturing test costs at a level that allows for reasonable selling prices even for complex products utilizing the latest silicon technologies The book is structured into three parts The first part provides a summary of DfT techniques and an introduction to pattern generation techniques The second part delves into established DfT techniques for special analogmixed signal circuits and memories within the industry The third part proposes a systematic approach to test concept engineering maximizing the

benefits of DfT methodologies By exploring the fundamentals and advanced concepts of DfT this book aims to equip readers with the knowledge and tools necessary to contribute to the ongoing innovation in semiconductor testing and development

Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Sandeep K. Goel, Krishnendu

Chakrabarty, 2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs However the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations power supply noise crosstalk resistive opens bridges and design for manufacturing DfM related rule violations The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non critical paths in the circuit Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on alternative methods that explores new metrics top off ATPG and circuit topology based solutions Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement Written from the triple viewpoint of university researchers EDA tool developers and chip designers and tool users this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective The book is designed as a one stop reference for current industrial practices research challenges in the domain of SDD testing and recent developments in SDD solutions **High**

Quality Test Pattern Generation and Boolean Satisfiability Stephan Eggersgluß, Rolf Drechsler, 2012-02-01 This book provides an overview of automatic test pattern generation ATPG and introduces novel techniques to complement classical ATPG based on Boolean Satisfiability SAT A fast and highly fault efficient SAT based ATPG framework is presented which is also able to generate high quality delay tests such as robust path delay tests as well as tests with long propagation paths to detect small delay defects The aim of the techniques and methodologies presented in this book is to improve SAT based ATPG in order to make it applicable in industrial practice Readers will learn to improve the performance and robustness of the overall test generation process so that the ATPG algorithm reliably will generate test patterns for most targeted faults in acceptable run time to meet the high fault coverage demands of industry The techniques and improvements presented in this book provide the following advantages Provides a comprehensive introduction to test generation and Boolean Satisfiability SAT Describes a highly fault efficient SAT based ATPG framework Introduces circuit oriented SAT solving techniques which make use of structural information and are able to accelerate the search process significantly Provides SAT formulations for the prevalent delay faults models in addition to the classical stuck at fault model Includes an industrial perspective on the state of the art in the testing along with SAT two topics typically distinguished from each other

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