

Total No. of Questions : 8]

SEAT No. :

PA-1237

[Total No. of Pages : 2

[5925]-259

S.E. (Computer Engineering)

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2019 Pattern) (Semester - III) (210245)

Time : 2½ Hours]

[Max. Marks : 70

Instructions to the candidates:

- 1) Attempt Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Assume suitable data, if necessary.

Q1) a) What are sequential circuits? Explain excitation table of JK flipflop. [6]

b) Convert Following Flipflops: [6]

i) SR to JK

ii) JK to D

c) What is MOD counter? Design MOD - 24 counter using 7490. [6]

OR

Q2) a) What are sequential circuits? Explain SR flipflop using a suitable example. [6]

b) Convert Following Flipflops: [6]

i) JK to T

ii) SR to D

c) Design sequence detector using MS JK flipflop for sequence 1101. [6]

Q3) a) Draw ASM chart for 2-bit UP counter using multiplexer controller method. [6]

b) Draw a block diagram of the PLA device and explain. [6]

c) Implement following Boolean function using PAL. [5]

$$F1 = \sum m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$$

$$F2 = \sum m(1, 2, 8, 12, 13)$$

OR

P.T.O.

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